ACBEL POLYTECH INC.

ERP1U 300W

1U 1+1 Redundant Distribution Board Specification

Model Number: R1BU5301B-G Series
AcBel PN: FSD002 Series

use R1Bb Module Series

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Changed by: Johnny Ho

REVISION LOG

DATE	SECTION	REVISION	ISSUE / DESCRIPTION
2014/12/22		S00	Draft release
2015/03/02	All	S01	General update
2105/05/13	2.3.2	S02	Update -12V regulation
	3		Add -12V PG delay time
	5.1		Update main output OCP range

1. GENERAL SCOPE

This specification describes the performance characteristic of a DC-DC switching power distribution board (PDB) with a +12V main DC input and a +5Vsb auxiliary input. The PDB will switch into +5V, +3.3V, -12V main and +5Vsb auxiliary output and distribute +12V main output. The PDB operates with a single power supply or in N+1 parallel. Power modules shall support hot-plug and active load share for 12V Main output. Mixed operation of different input type power modules (AC-DC and DC-DC) is allowed. The PDB shall limit the OPP to 300W continuous power operation.

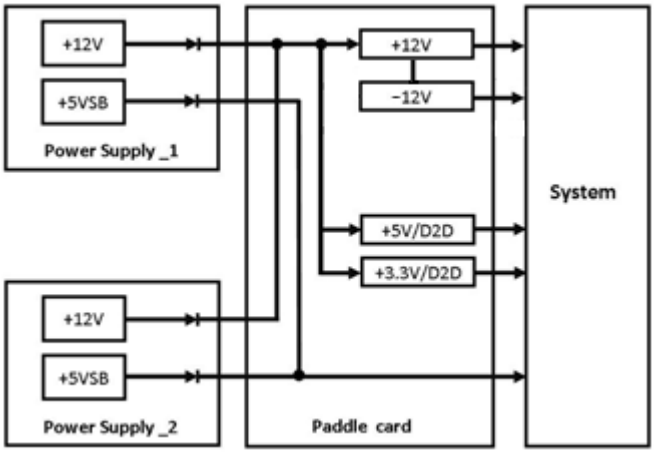


Figure 1- General Architecture

2. ELETRICAL PERFORMANCE

2.1 POWER BUS AND SIGNAL CONNECTOR

The PDB shall have a common Power Bus and signal connector complying with Molex interconnects series. The exact PN for interconnect is **Molex PN 45984-4143 or equivalent.**

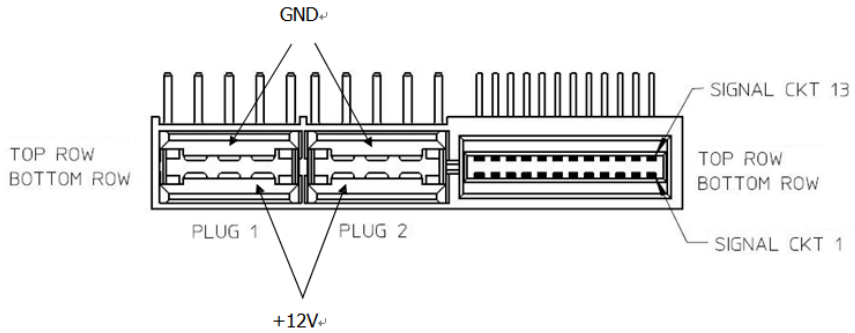


Figure 2 – PDB Connector – PDB sides.

The Pin definition shall comply with table 1 below and shall provide 12VDC as main input and 5VsbDC as auxiliary input.

PSU DC +12V output is on the bottom set of 2 power pins (blades). And PSU DC GROUND is on the top set of 2 power pins (blades). The +12V pins should touch last and break first and

the DC GROUND pins should touch first and break last when the PSU is mated to the PDB connector.

The PSU must have tabs on its card edge to mate with the PDB connector, similar to that shown in the following figure.

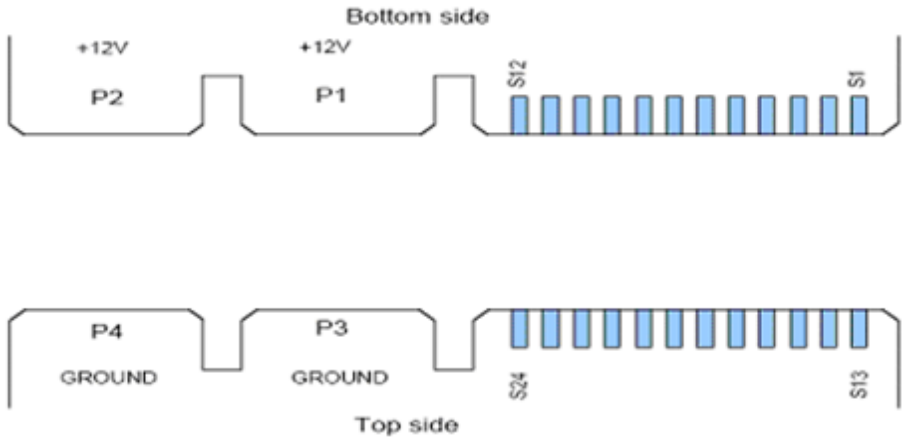


Figure 3 – Golden finger – PSU sides (Top View)

Table 1 - Input connector pin assignment:

Pin Name	Signal Name	Function	Pin Name	Signal Name	Function
P1 & P2	Main_Output (MO+)	+12V (Bottom)	S13	N/C	N/C
P3 & P4	RTN (GND)	+12V return (Top)	S14	Present#	PS present
S1	Remote Sense (+)	+12VS	S15	A0	I^2C address bit 0
S2	Remote Sense (-)	+12V RTN Sense	S16	N/C	N/C
S3	12LS	Current share bus	S17	N/C	N/C
S4	SMB_Alert	Failure notification	S18	EEPROM	EEPROM_WP
S5	SDA	I^2C Data signal	S19	Input_OK#	Input present signal
S6	SCL	I^2C Clock signal	S20	N/C	N/C
S7	N/C	N/C	S21	CR	Cold Redundant
S8	PSON	Power enable input	S22	N/C	N/C
S9	PWOK	Power output	S23	+5Vsb	+5Vsb output
S10	A1	I^2C address bit 1	S24	+5Vsb	+5Vsb output
S11	+5Vsb	+5Vsb output			
S12	+5Vsb	+5Vsb output			

Notes:

1. The +3.3V/+5V/+12V/-12V derives their power from +12V.
2. PDB will pass $+5V_{SB}$ to system.
3. See section 6, “Signal Definition”

2.2 POWER INPUT SPECIFICATION

2.2.1 Input Voltage

The maximum input current defines the maximum possible input current to ensure the proper function of the PDB to meet all defined specifications.

INPUT VOLTAGE	INPUT CURRENT	MAX POWER
12VDC	24A	288W
$5V_{SB}$ DC	2.5A	12.5W

2.2.3 Efficiency

The D2D converter shall have at least an efficiency rating in the table below:

Load	Minimum Efficiency	
	+5V	+3.3V
20%	92%	90%
50%	94%	92%
100%	93%	91%

2.2.3.1 Efficiency of multi-output power system

The efficiency of multi-output power system should be measured at 230VAC with following criteria and meet the efficiency requirements:

Configuration	Load	Minimum Efficiency
1+0	20%	80%
1+1	50%	80%

2.3 POWER OUTPUT SPECIFICATION

2.3.1 Output Power/Currents

The following table defines the power and current rating of a PDB, which supports up to combined 300W output power and power module output limitation. The combined output power of all outputs shall not exceed the rated output power. The power supply system must meet both static and dynamic voltage regulation requirements.

The maximum combined steady output power shall follow by below table, no matter how the current draw will be combined.

Output Current Table:

Voltage	Mini	Max
+3.3V	0.1A	15A
+5V	0.1A	18A
-12V	0.0A	0.3A
+12V	follow PSU	24A
+5Vsb	follow PSU	follow PSU

1. Maximum continuous total DC output power should not exceed 300W.
2. The +3.3V/+5V/+12V/-12V derives their power from +12V.

2.3.2 Voltage Regulation

The power supply shall stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise conditions specified in paragraph 2.2.5. All outputs are measured with reference to the return remote sense (ReturnS) signal.

Parameter	MIN	NOM	MAX	Units	Tolerance
+3.3V	+3.13	+3.30	+3.47	V_{rms}	+/-5%
+5V	+4.75	+5.00	+5.25	V_{rms}	+/-5%
+12V	+11.40	+12.00	+12.60	V_{rms}	+/-5%
-12V	-11.40	-12.00	-13.20	V_{rms}	+10/-5%
+5Vsb	+4.75	+5.00	+5.25	V_{rms}	+/-5%

2.3.3 Dynamic Loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

Output	△Step Load Size	Load Slew Rate	Capacitive Load
+3.3V	30% of max load	o.5 A/μs	470 μF
+5V	30% of max load	o.5 A/μs	470 μF
+12V	30% of max load	o.5 A/μs	470 μF
+5Vsb	30% of max load	o.5 A/μs	10 μF

2.3.4 Capacitive Loading

The power supply shall meet all requirements with the following capacitive loading ranges.

Output	MIN	MAX	Units
+3.3V	470	8,000	μF
+5V	470	8,000	μF
+12V	follow PSU	follow PSU	μF
+5Vsb	follow PSU	follow PSU	μF

2.3.5 Ripple and Noise

Ripple and Noise shall be measured over a Bandwidth of 20MHz at the power supply output connector. A 0.1μF ceramic capacitor and 10μF of tantalum capacitor shall be placed at each point of measurement.

+3.3V	**+5V**	**-12V**	**+12V**	**+5Vsb**
50 mVp-p	50 mVp-p	120mVp-p	follow PSU	follow PSU

2.3.6 Maximum Load Change

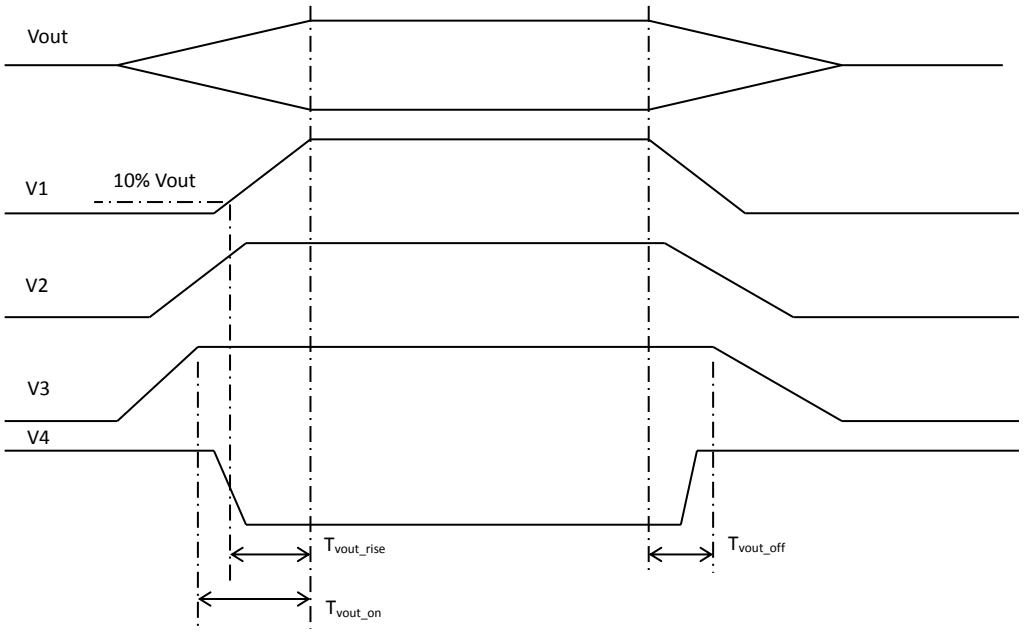
The power supply shall continue to operate normally when there is a step change ≤ 1 A/μsec between minimum load and maximum load.

3. TIMING SEQUENCE

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 70ms. For 5Vsb, it is allowed to rise from 1 to 25ms. All main outputs shall rise positive monotonically and have a slop value between 0 V/mS to 0.1V/mS.
For 5Vsb output any 5ms segment of the 10% to 90% rise time waveform, a straight line draw between the end points of the waveform segment must have s slope ≥ [Vout, nominal /20]V/mS.
Each output voltage shall reach regulation within 5mS (Tvout_on) of each other during turn on of the power supply system. Each output voltage shall fall out of regulation within 400mS (Tvout_off) of each other during turn off.
Table below shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

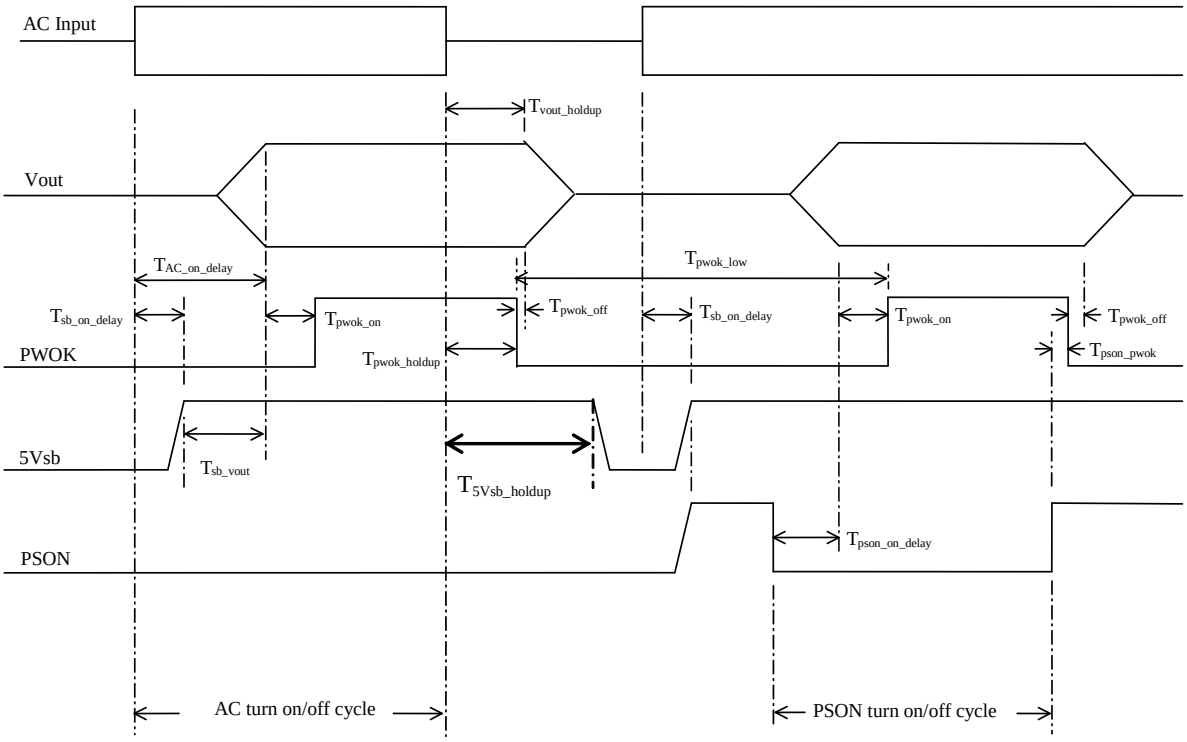
Item	**Description**	**MIN**	**MAX**	**Units**
Tvout rise	Output voltage rise time for all main output	5	70	ms
	Output voltage rise time for the 5Vsb output	1	25	ms
Tvout_on	All main outputs must be within regulation of each other within this time.		50	ms
Tvout_off	All main outputs must leave regulation within this time.		400	ms

Output Voltage Timing



Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
T sb_on_delay	Delay from ac begin applied to 5Vsb begin within regulation.		1500	ms
T ac_on_delay	Delay from AC begin applied to all output voltage begin within regulation.		2500	ms
T out_holdup	Time all output voltages stay within regulation after loss of AC.	12		ms
T pwok_holdup	Delay from loss of AC to de-assertion of PWOK.	10		ms
T pson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# de-active to PWOK begin de-asserted.		50	ms
T pwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T pwok_off	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
T psok_low	Duration of PWOK begin in the de-asserted state during an off/on cycle using AC or the PSON# signal.	100		ms
T sb_vout	Delay from 5Vsb begin in regulation to O/Ps begin in regulation at AC turn on.	50	1000	ms



4. CONTROL AND INDICATOR FUNCTIONS

The following section defines the input and output signals from the power supply. Signals that can be defined as low true use the following convention:
Signal# = low true.

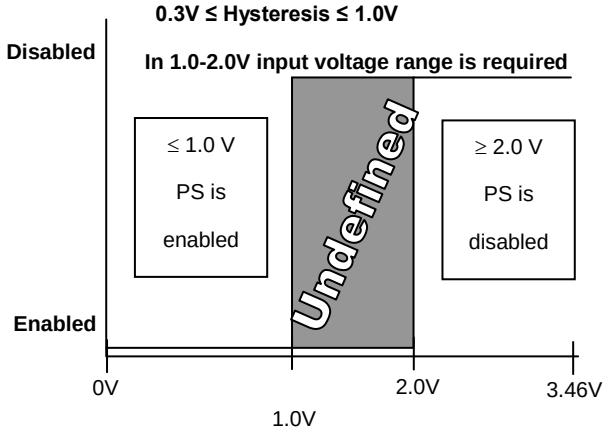
4.1 PSON# INPUT SIGNAL (POWER SUPPLY ENABLE)

The PSON# signal is required to remotely turn on/off the main output of the power supply. PSON# is an active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply.

PSON# Signal Characteristic

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to VSB located in the power supply**.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, V_{pson} = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms
T_{pson} = Delay PSON# disconnect MO OFF		100µsec

PSON# Signal Characteristic



4.2 POWER OK (PWOK OR PG) BUS

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

PWOK / PG Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**
Logic level low voltage, I_{sink} = 4mA	0V	0.4V
Logic level high voltage, I_{source} = 200µA	2.4V	3.46V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: T_{pwok_off}	1ms	200ms

4.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

SMBAlert# signal characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	**MAX**
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{sink} = 50µA	2.4V	3.46V
Sink current, Alert#=low		4mA
Sink current, Alert#=high		50µA
50µA rise and fall time		100µsec
SmaRT input power fail assertion		2msec
Thermal CLST ΔT to critical thermal	10°C	

5. PROTECTION CIRCUITS

Protection circuits inside the PDB shall cause only the main output to shutdown (latch off). If the power supply latches off due to a protection circuit assert, an Input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

Specific protection circuits shall not latch, but auto recover when the latching reason had been cleared. This protection circuits will be written in cursive writing and will have an Auto Recover ($Output_{Ar}$) in the chapter name.

The auxiliary output shall not affect by any protection circuit, unless the auxiliary output itself is affected.

5.1 CURRENT LIMIT

The power supply shall prevent the main and auxiliary outputs from exceeding the values shown in below Table. If the main current limits are exceeded the power supply will shut down and latch off, *the auxiliary output shall be auto recover* ***(Vsb_{AR})*** *after the OCP had been removed.*

The PDB shall alert the system of the OCP condition via SMBAlert#.

Over Current Protection

Voltage	**Over Current Limit (Iout limit)**
+3.3V	110% - 150% maximum
+5V	110% - 150% maximum
+12V	110% - 150% maximum
+5Vsb ***(Auxiliary)AR****	follow PSU module *NOTE

Note: +5Vsb for PDB was a pass through design, in single power module had maximum 6A limit.

5.2 OVER VOLTAGE PROTECTION

The power supply shall shutdown and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption.

The PDB shall alert the system of the OVP condition via SMBAlert#.

Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	3.6	4.5
+5V	5.55	6.55
+12V	follow PSU	follow PSU
+5Vsb ***(Auxiliary)AR***	follow PSU	follow PSU

Note: +12V OVP is set 14.5V; +5Vsb is 6.5V

5.3 UNDER VOLTAGE PROTECTION

The power supply shall shutdown and latch off after an under voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption.

The PDB shall alert the system of the UVP condition via SMBAlert#.

The +3.3V/+5V/+12V/+5Vsb UV setting as below:

Under Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	2.3	3
+5V	3.5	4.4
+12V	follow PSU	follow PSU
+5Vsb ***(Auxiliary)AR***	follow PSU	follow PSU

5.4 SHORT CIRCUIT PROTECTION

The power supply shall shutdown and latch off after an under voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption.

The PDB shall alert the system of the SCP condition via SMBAlert#.

Short Circuit Protection

Voltage	Min Short Circuit Threshold
+3.3V	30A
+5V	30A
+12V	follow PSU
+5Vsb ***(Auxiliary)AR****	follow PSU

5.5 RESTART AFTER LATCH OFF

Restart can be accomplished in one of two ways:

1. By toggling the PDB_ON# signal from active to inactive to active. The duration of inactive time should be longer than 10 msec.
2. By removing all PSUs for at least 1 second. And then plug PSU in.

6. SIGNAL DEFINITION

6.1 PDB_ON#

The PDB_ON# is an open collector active low output signal of system, and it is an input signal of PDB. System controls PDB on or off via this signal. When the signal is active, PDB will turn on. When the signal is inactive, PDB will shut down.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2V or higher.

System must not pull this signal up.

6.2 PSU_ON#

The PSU_ON# is a logic low output signal of PDB, and it is an input signal of PSUs. Two PSU's PSU_ON# pins are wired together by PDB. PDB controls PSUs On or Off via this signal. When this signal is high, the PSU output will turn On is PSU AC input is ready. When this signal is low, the PSU output will turn Off.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if this level is 2V or higher.

PSU must pull this signal up via 10K~47Kohm

6.3 PDB_OK

The PDB_OK is a logic high output signal of PDB, and it is an input signal of system. When PDB status is OK, PDB_OK signal will be high. When PDB status is not OK, PDB_OK signal will be low.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2V or higher.

System must pull this signal up via 10K~47Kohm

6.4 PSU_OK

The PSU_OK is an open collector output of PDU, and it is a logic high signal of PDB. It used to indicate the PDU status. When PDU status is OK, PSU_OK signal will be pull high to PDB internal bias. When PSU status is not OK, PDB_OK signal will be active low.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2V or higher, PSU must not pull this signal up.

6.5 AC_OK

The AC_OK is an open collector output of PSU, and it is a logic high input of PDB. It used to indicate the PSU AC status. When PSU AC status is OK, AC_OK signal will be pull high to PDB internal bias. When PSU status is not OK, AC_OK signal will be active low.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2V or higher.

PSU must not pull this signal up.

6.6 PRESENT#

The PRESENT# is logic low input of PDB, and it is an output of PSU. It used to indicate the PSU's presence. The PSU wires this signal to ground.

PSU must wire this signal to ground.

6.7 12VRS+ & 12VRS-

The 12VRS+ and 12VRS- were for +12V remote sensing. PDB wires these two signals to +12V and GND of output connector terminals for voltage compensation.

6.8 3.3VRS+ & 5VRS+

The 3.3VRS+ and 5VRS+ were for +3.3V and +5V remote sensing. PDB wires these two signals to +3.3V and +5V output connector terminals voltage compensation.

6.9 12VLS

12VLS is 12V current sharing bus of active-current-sharing method. Two PSU's 12VLS pins are wired together by PDB, and PSUs will equalize 12V output load by this signal.

If PSU doesn't support active-current-sharing method, PSU must left this pin open.

6.10 SERIAL BUS COMMUNICATION

The PDB will communicate with system by serial bus. The buses are compatible with Vdd =3.3V,

100kHz, and SMBus 2.0 'high power'. The following signals will be used for this communication.

System must pull these pins to 3.3V.

6.11 SMBus_Clock

Bi-directional signal used to synchronize communications. The SMBus_Clock pins of PDB, PSU and system should be wired together.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2.1V or higher.

System must pull this signal up via 10k~47kohm. PSU must not pull this signal up.

6.12 SMBus_Data

Bi-directional signal used to synchronize communications. The SMBus_Data pins of PDB, PSU and system should be wired together.

This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2.1V or higher.

System must pull this signal up via 10k~47kohm. PSU must not pull this signal up.

6.13 PSU_SMBUS_Alert# & PDB_SMBUS_Alert#

PSU_SMBus_Alert# is generated by the PSU whenever it experiences a problem that the system should know about. PDB_SMBus_Alert# is a logical AND of two PSUs' PSU_SMBus_ Alert#. Any problem experienced by the PSU or PDB will cause PDB_SMBus_Alert# to assert.

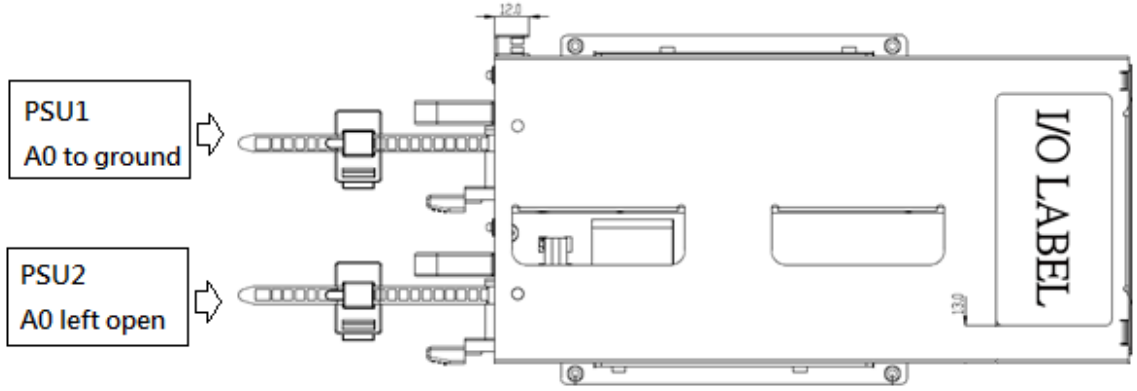
This signal is considered logically low if its level is 0.8V or less. It is considered logically high if its level is 2.1V or higher.

System must pull this signal up via 10k~47kohm. PSU must not pull this signal up.

6.14 A0

A0 is a signal to set up PSU serial bus address. The PSU must pull this signal up via 10k~47k ohm. A0 pin of PSU1 will be wired to ground by PDB. And A0 pin of PSU2 will be left open.

The setting is as following picture



7. SERIAL BUS COMMUNICATION

7.1 STATUS AND FAULT INFORMATION

The commands in the following table are system read only.

Status Command Code

Command Code	Command Name	bit	Status
F0h	MFR_SPECIFIC_32	5	AC_OK_PSU2
		4	AC_OK_PSU1
		3	PSU_OK_PSU2
		2	PSU_OK_PSU1
		1	PRESENT#_PSU2
		0	PRESENT#_PSU1
		4	3.3V_Iout OC Fault
		3	5V_Iout OC Fault
		0	12V_Iout OC Fault
		4	3.3V_Vout UV Fault
		3	5V_Vout UV Fault
		2	Reserve
		1	3.3V_Vout OV Fault
		0	5V_Vout OV Fault

Status Information

I2C STATUS	STATUS GOOD	STATUS Fail
AC_OK_PSU2	bit=1	bit=0
AC_OK_PSU1	bit=1	bit=0
PSU_OK_PSU2	bit=1	bit=0
PSU_OK_PSU1	bit=1	bit=0
PRESENT#_PSU2	bit=1	bit=0
PRESENT#_PSU1	bit=1	bit=0

8. ENVIRONMENTAL

8.1 TEMPERATURE REQUIREMENTS

The power supply shall operate within all specified limits over the Top temperature range. The average air temperature difference ($\triangle T_{ps}$) from the inlet to the outlet of the power supply shall not exceed the values shown below Table. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply

ITEM	DESCRIPTION	MIN	MAX	UNITS
T_{op}	Operating temperature range.	0	45	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	60	°C

8.2 HUMIDITY

Operating: 20% to 85% relative humidity, non-condensing.
Storage: 10% to 90% relative humidity, non-condensing.

8.3 ALTITUDE

Operating: to 10,000ft (3,050m)
Non-operating: to 25,000ft

8.4 VIBRATION

Operating: 0.01G2/Hz at 10Hz, 0.02G2/Hz at 20Hz.
Non-Operating: 0.02G2/Hz form 20Hz to 1000Hz.

8.5 MECHANICAL SHOCK

Operating: 5G, no malfunction.
Non-operating: 50G, no damage. Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

8.6 EMI/EMC REQUIREMENTS

The power supply shall comply with FCC part 15, CRISP 22 and EN55-22; Class A for both conducted and radiated emissions with a 6dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Tests will be performed full load on each output power at 120VAC, 60Hz, and 230VAC, 50Hz.

9. REGULATORY REQUIREMENTS

9.1 PRODUCT SAFETY COMPLIANCE

The PDB shall meet following safety regulation with most current editions:

A) UL 60950-1/CSA 60950-1 Edition 2 (USA/Canada)
B) TUV EN60950-1 Edition 2 (Europe)
C) IEC60950-1 Edition 2 (International)
D) CB Certificate & Report, IEC60950-1 Edition 2
E) CE – Low Voltage Directive 2006/95/EC (Europe)
F) BSMI (Taiwan)
G) GB4943-2011 Certification (China)

10.RELIABILITY

The MTBF of the power supply can be calculated with the Part-Stress Analysis method of Bell Core SR-332 Issue 1 using the quality factors. A calculated MTBF of the power supply shall be at least 100,000 hours at 40°C ambient with 115VAC and in 80% load condition.

11. RoHS COMPLIANCE

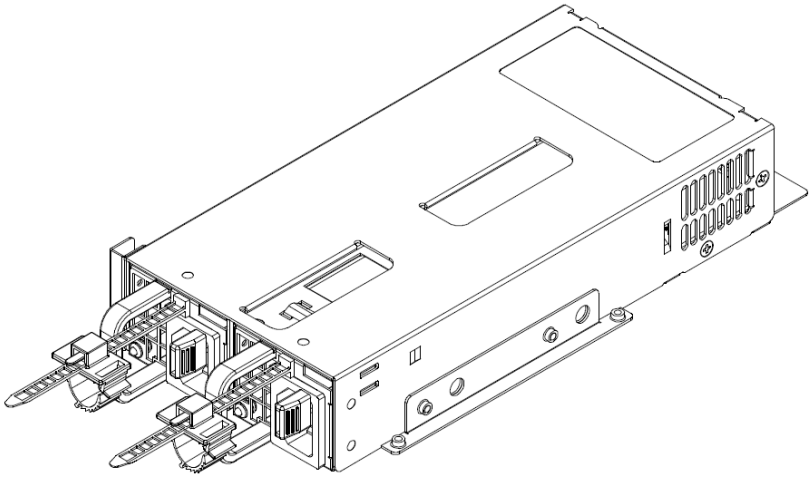
The directive 2002/95/EC of the European Parliament and of the Council of the 27th January 2003, on the restriction of the use of certain hazardous substances in electrical and electronic equipment, requires the reduction of the substances Lead, Mercury, Cadmium, Hexavalent Chromium, Polybrominated Biphenyls (PBB), and Polybrominated Biphenyl ethers (PBDE) in electronic products by July 1, 2006. Unless otherwise noted, all materials used will be compliant with this directive and any subsequent revisions or amendments.

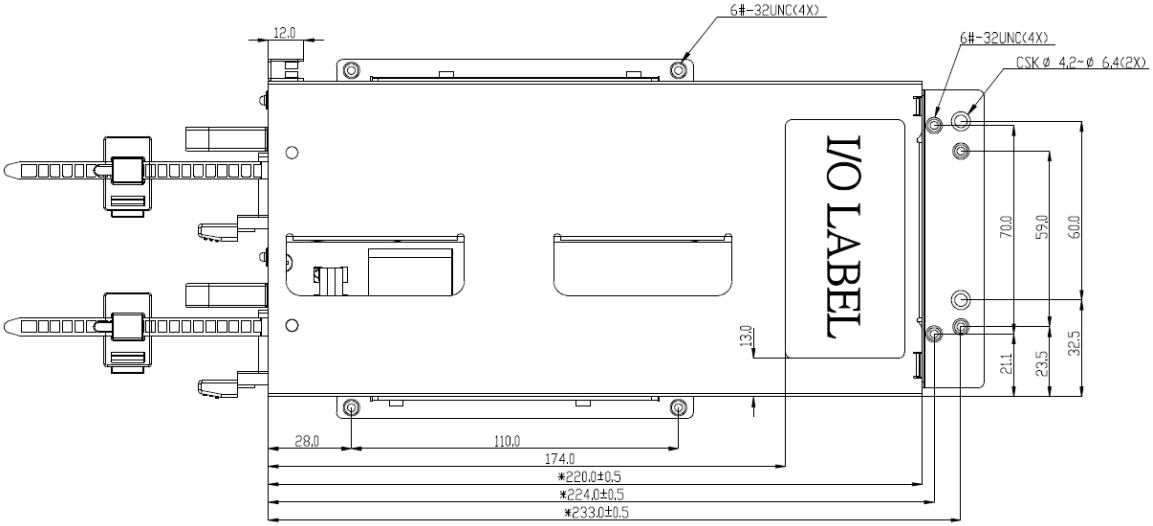
12. MECHANICAL DIMENSIONS

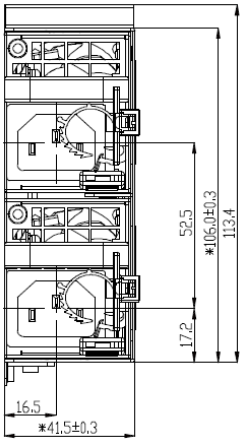
12.1 POWER SYSTEM DIMENSIONS

Dimension (L x W x H): 220 x 106 x 41.5mm / 8.66 x 4.17 x 1.63inch

Note: Bracket is an optional item upon request.





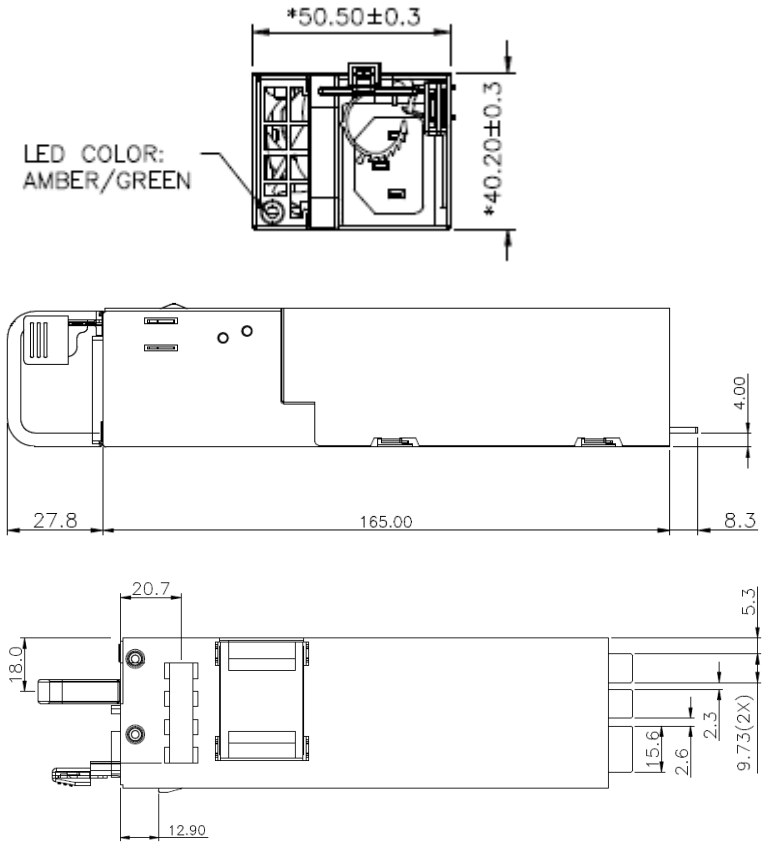


12.2 OUTPUT CABLE DIAGRAM

Please refer to detail mechanical drawing

12.3 POWER MODULE DIMENSIONS

Dimension (L x W x H): 165 x 50.5 x 40.2mm / 6.50” x 1.99” x 1.59”inch



<for reference only, detail drawing MUST use from MO file>